UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,937	05/10/2001	David M. Blaker	9269-5	5828

20792 7590 12/08/2004		

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EXAMINER
LANIER, BENJAMIN E

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	09/852,937	BLAKER ET AL.
Office Action Summary	Examiner	Art Unit	
	Benjamin E Lanier	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

    4a) Of the above claim(s) *9-15,24-26 and 35-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 16-23, 27-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *5/16,4/5,3/14,2/6.*

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1.   Restriction to one of the following inventions is required under 35 U.S.C. 121:

      I.   Claims 1-8, 16-23, 27-34, drawn to a first method of operating a cryptographic

              data processing system, classified in class 713, subclass 190.

      II.   Claims 9-15, 24-26, 35-40, drawn to a second method of operating a

              cryptographic data processing system, classified in class 713, subclass 189.

2.   The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single

combination. The subcombinations are distinct from each other if they are shown to be

separately usable. In the instant case, invention I has separate utility such as executing an

instruction that references at least one operand located in local memory. Invention II has separate

utility such as executing a plurality of command blocks using the plurality of execution units.

See MPEP § 806.05(d).

3.   Because these inventions are distinct for the reasons given above and have acquired a

separate status in the art as shown by their different classification, restriction for examination

purposes as indicated is proper.

4.   Because these inventions are distinct for the reasons given above and the search required

for Group I is not required for Group II, restriction for examination purposes as indicated is

proper.

5.   Because these inventions are distinct for the reasons given above and have acquired a

separate status in the art because of their recognized divergent subject matter, restriction for

examination purposes as indicated is proper.

6.   During a telephone conversation with Scott Moore on 15 November 2004 a provisional

election was made without traverse to prosecute the invention of Group I, claims 1-8, 16-23, 27-

34. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 9-15, 24-26, 35-40 withdrawn from further consideration by the examiner, 37

CFR 1.142(b), as being drawn to a non-elected invention.

7.   Applicant is reminded that upon the cancellation of claims to a non-elected invention, the

inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the

currently named inventors is no longer an inventor of at least one claim remaining in the

application. Any amendment of inventorship must be accompanied by a request under 37 CFR

1.48(b) and by the fee required under 37 CFR 1.17(i).

Double Patenting

8.   The nonstatutory double patenting rejection is based on a judicially created doctrine
grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or
improper timewise extension of the "right to exclude" granted by a patent and to prevent possible
harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.
Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686
F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA
1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
        A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to
overcome an actual or provisional rejection based on a nonstatutory double patenting ground
provided the conflicting application or patent is shown to be commonly owned with this
application. See 37 CFR 1.130(b).
        Effective January 1, 1994, a registered attorney or agent of record may sign a terminal
disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37
CFR 3.73(b).

9.   Claims 1, 4, 6, 7, 16, 19, 21, 22, 27, 30, 32, 33 are provisionally rejected under the

judicially created doctrine of obviousness-type double patenting as being unpatentable over

claims 1, 3, 31, 59 of copending Application No. 09/852,562. Although the conflicting claims

are not identical, they are not patentably distinct from each other because A method of operating

a cryptographic data processing system that comprises a host processor, a system memory

coupled to the host processor, and a cryptographic processor integrated circuit that comprises a

local memory and is coupled to the host process and the system memory, the method comprising:

loading at least one operand from the system memory to the local memory; performing at least

one operation on the at least one operand to generate a result in the local memory; and storing the

result generated in memory. The difference being that the result in the instant application is

stored at a second relative position in the local memory whereas the result in the '562 reference

is stored in system memory.

        This is a provisional obviousness-type double patenting rejection because the conflicting

claims have not in fact been patented.

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

11.   Claims 1-3, 5, 6, 8, 16-18, 20, 21, 23, 27-29, 31, 32, 34 are rejected under 35

U.S.C. 102(e) as being anticipated by Moyer, U.S. Patent No. 6,327,647. Referring to claims 1,

6, 16, 21, 27, 32, Moyer discloses a method for interfacing a host processor, with memory (Fig.

1), and a co-processor, with memory (Abstract & Fig. 1), wherein the co-processor is a

cryptographic processor (Col. 1, lines 45-48), which meets the limitation of operating a

cryptographic system that comprises a host processor, a system memory coupled to the host

processor, and a cryptographic processor integrated circuit that comprises a local memory and is

coupled to the host processor and the system memory. The cryptographic processor loads an

operand from system memory into local memory to execute an instruction using the operand

(Col. 8, line 56 – Col. 9, line 8), which meets the limitation of loading at least one operand from

the system memory to the local memory and executing an instruction using the cryptographic

processor that references the at least one operand using a first relative position in the local

memory.

        Referring to claims 2, 17, 28, Moyer discloses moving several operands into memory

(Col. 12, lines 49-63), which meets the limitation of loading at least one operand from the system

memory to the local memory comprises at least two operands and executing the instruction using

the cryptographic processor that references a first one of the operands using the first relative

position in the local memory and a second one of the operands using a second relative position in

the local memory, the first and second relative positions being contiguous with one another.

        Referring to claims 3, 18, 29, Moyer discloses that the operands have different sizes (Col.

12, lines 13-14), which meets the limitation of the operands comprising a different number of

bits.

Referring to claims 5, 8, 20, 23, 31, 34, Moyer discloses that the relative memory

positions comprise an offset from a base address in the local memory (Col. 12, lines 53-57).

Referring to claims 4, 7, 19, 22, 30, 33, Moyer discloses producing an output as result of

executing instructions and subsequently storing the output in memory (Col. 4, line 33 – Col. 5,

line 12), which meets the limitation of generating a result based on the at least one operand and

storing the result at a second relative position in the local memory.

Conclusion

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Benjamin E Lanier whose telephone number is 703-305-7684.

The examiner can normally be reached on M-Th0 7:30am-5:00pm, F 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Gilberto Barron can be reached on (703)305-1830. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin E. Lanier

THOMAS R. PEESO
PRIMARY EXAMINER